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Design Automation Conference 1997. Proceedings of the ASP-DAC '97. Asia and South Pacific , 28-31 Jan. 1997

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7 Experiments with a performance driven module generator

Kim, S.; Owens, R.M.; Irwin, M.J.;

Design Automation Conference, 1992. Proceedings., 29th ACM/IEEE , 8-12 Jun 1992

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1 A high performance SI memory cell

Leenaerts, D.M.W.; Leeuwenburgh, A.J.; Persoon, G.G.;
 Circuits and Systems, 1994., Proceedings of the 37th Midwest Symposium on , Volume: 1 , 3-5 Aug. 1994
 Pages:38 - 41 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(556 KB\)\]](#) IEEE CNF

2 An efficient symbolic approach to time delay optimization of CMOS circuits

Styblinski, M.A.; Sun, X.; Opalska, K.M.; Opalski, L.J.;
 Circuits and Systems, 1991., IEEE International Symposium on , 11-14 June 1
 Pages:814 - 817 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(304 KB\)\]](#) IEEE CNF

3 Memory generator method for sizing transistors in RAM/ROM blocks

Donnelly, D.;
 Memory Technology, Design and Testing, 1998. Proceedings. International Workshop on , 24-25 Aug. 1998
 Pages:10 - 11

[\[Abstract\]](#) [\[PDF Full-Text \(12 KB\)\]](#) IEEE CNF

4 A method for sizing transistors in CMOS op-amps

Smith, M.H.; Walczowski, L.T.; Waller, W.A.J.; Howard, D.;
 Circuits and Systems, 1991., IEEE International Symposium on , 11-14 June 1
 Pages:2016 - 2019 vol.4

[\[Abstract\]](#) [\[PDF Full-Text \(272 KB\)\]](#) IEEE CNF

5 Technology for advanced high-performance microprocessors*Bohr, M.T.; El-Mansy, Y.A.;*

Electron Devices, IEEE Transactions on , Volume: 45 , Issue: 3 , March 1998

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6 Power-delay characteristics of CMOS adders*Nagendra, C.; Owens, R.M.; Irwin, M.J.;*

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume:

2 , Issue: 3 , Sept. 1994

Pages:377 - 381

[\[Abstract\]](#) [\[PDF Full-Text \(408 KB\)\]](#) IEEE JNL

7 Numerical simulation of hard errors induced by heavy ions in 4T high density SRAM cells*Gaillard, R.; Poirault, G.;*

Nuclear Science, IEEE Transactions on , Volume: 41 , Issue: 3 , Jun 1994

Pages:613 - 618

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8 A novel wide-band CMOS current amplifying cell and its application power supply current monitoring*Dragic, S.; Filanovsky, I.M.; Margala, M.;*

Electronics, Circuits and Systems, 2001. ICECS 2001. The 8th IEEE International Conference on , Volume: 1 , 2-5 Sept. 2001

Pages:27 - 30 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(312 KB\)\]](#) IEEE CNF

9 Automated transistor sizing algorithm for minimizing spurious switching activities in CMOS circuits*Wroblewski, A.; Schimpfle, C.V.; Nossek, J.A.;*

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Pages:291 - 294 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(328 KB\)\]](#) IEEE CNF

10 Reaching the limits of CMOS technology*Isaac, R.D.;*

Electrical Performance of Electronic Packaging, 1998. IEEE 7th topical Meeting on , 26-28 Oct. 1998

Pages:3

[\[Abstract\]](#) [\[PDF Full-Text \(76 KB\)\]](#) IEEE CNF

11 Modeling and layout optimization of VLSI devices and interconnect deep submicron design*Cong, J.;*

Design Automation Conference 1997. Proceedings of the ASP-DAC '97. Asia a
South Pacific , 28-31 Jan. 1997
Pages:121 - 126

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1992

Pages:687 - 690

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1 A mixed-clock issue queue design for globally asynchronous, locally synchronous processor cores

Rapaka, V.S.P.; Marculescu, D.;

Low Power Electronics and Design, 2003. ISLPED '03. Proceedings of the 2003 International Symposium on , 25-27 Aug. 2003

Pages:372 - 377

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2 An asynchronous FIFO with fights: case study in speed optimization

Laberge, S.; Negulescu, R.;

Electronics, Circuits and Systems, 2000. ICECS 2000. The 7th IEEE International Conference on , Volume: 2 , 17-20 Dec. 2000

Pages:755 - 758 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(300 KB\)\]](#) IEEE CNF

3 Stochastic cycle period analysis in timed circuits

Mercer, E.G.; Myers, C.J.;

Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on , Volume: 2 , 28-31 May 2000

Pages:172 - 175 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(348 KB\)\]](#) IEEE CNF

4 DUES: a fault abstraction and collapsing framework for asynchronous circuits

Shirvani, P.P.; Mitra, S.; Ebergen, J.C.; Roncken, M.;

Advanced Research in Asynchronous Circuits and Systems, 2000. (ASYNC 2000 Proceedings. Sixth International Symposium on , 2-6 April 2000

Pages:73 - 82

[\[Abstract\]](#) [\[PDF Full-Text \(184 KB\)\]](#) IEEE CNF

5 Verification of delayed-reset domino circuits using ATACS

Belluomini, W.; Myers, C.J.; Hofstee, H.P.;

Advanced Research in Asynchronous Circuits and Systems, 1999. Proceedings Fifth International Symposium on , 19-21 April 1999

Pages:3 - 12

[\[Abstract\]](#) [\[PDF Full-Text \(144 KB\)\]](#) IEEE CNF

6 An asynchronous 2-D discrete cosine transform chip

Smith, R.; Fant, K.; Parker, D.; Stephani, R.; Ching-Yi Wang;

Advanced Research in Asynchronous Circuits and Systems, 1998. Proceedings 1998 Fourth International Symposium on , 30 March-2 April 1998

Pages:224 - 233

[\[Abstract\]](#) [\[PDF Full-Text \(104 KB\)\]](#) IEEE CNF

7 Self-timed 1-D ICT processor

Pang, J.T.C.; Choy, O.C.S.; Chan, C.F.; Cham, W.K.;

Design Automation Conference 1997. Proceedings of the ASP-DAC '97. Asia a South Pacific , 28-31 Jan. 1997

Pages:669 - 670

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